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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,255	03/07/2002	Yoshinori Ogawa	1248-0583P	9284

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2673	4

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,255	OGAWA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. Figures 12-13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of claims stated: "with respect to both a **data** signal line to be scanned **first** and a **data** signal line to be scanned **next**". It is not clear, how data lines could be scanned? The scanning usually done in horizontal direction and data presented on data lines at the time of scanning horizontal lines.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Udo et al. (Pub. No.; US 2002/0050972 A1).

As to claim 1, Udo et al. teaches an image display device (See page 1, paragraph 0002), comprising: a plurality of scanning signal lines (See Fig. 1, items G1-G4, page 2, paragraph 0036) and a plurality of data lines which crossing each other (See Fig. 1, items D1-D6, page 2, paragraph 0036) an electro-optical element (See Fig. 1, item C11), and a switching element (See Fig. 1, item T11) and a pixel capacitor (See Fig. 1, item C11) being provided in each pixel region (See Fig. 1, items G2, D2, page 1, paragraph 0036) surrounded by adjacent two of plurality of scanning lines (See Fig. 1, items G1, G3, page 1, paragraph 0036) and adjacent two of plurality of data signal lines (See Fig. 1, items D1, D3 page 1, paragraph 0036); a data signal driving circuit for outputting voltages in mutually reverse polarities with respect to a pair of adjacent pixels (See Figs. 1, 2A, items 10, +-, page 2, paragraph 0040); and short-circuit means for short-circuiting respective pixel capacitors of pair of adjacent pixels (See Fig. 9, items D1-D2, S1, page 1, paragraph 0010) in non-selection period directly before a selection-scanning period of a target scanning signal line when scanning by switching polarities of the voltages (See Figs. 8-9, items D1-D2, S1, page 1, paragraphs 0007-0011) for gradation display (See page 1, paragraph 0002).

As to claims 2-3, 6, Udo et al. teaches data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to a pair pixels adjacent in a

direction of scanning, data signal lines and to adjacent frames (See Figs. 2A-2B, page 2, paragraph 0040).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Udo et al.

As to claim 4, Udo et al. teaches a positive voltage output section for outputting a positive voltage converted from a data signal (See Fig. 4, item PS1, page 3, paragraph 0054); and a negative voltage output section for outputting a negative voltage converted from a data signal (See Fig. 4, item NS1, page 3, paragraph 0054); a switching section for switching positive output section and negative output section between data signal lines (See Fig. 4, items P1-P2, N1-N2, page 3, paragraph 0055); wherein positive voltage output section negative voltage output section are used in common in data signal lines.

Udo et al. does not show adjacent data signal line.

Udo et al teaches adjacent signal line in Admitted Prior Art (APA) part (See Fig. 9, items D1-D2, S1, page 1, paragraph 0010).

It would have been obvious to one of ordinary skill in the art at the time of invention to use positive and negative voltage output sections in common in adjacent data signal lines as

shown by APA in Udo et al apparatus in order to reduce power consumption (See page 1, paragraph 0012 in Udo et al. reference).

As to claim 5, Udo et al. does not show positive voltage output section includes a positive polarity D/A converter and operational amplifier of N-channel MOS transistor input; and negative voltage output section includes a negative polarity D/A converter and operational amplifier of P-channel MOS transistor input.

Udo et al. teaches each of transfer gates has a PMOS and NMOS transistors connected in parallel to each other (See Figs. 5-6, items 21-22, page 3, 0057-0058).

It would have been obvious to one of ordinary skill in the art at the time of invention to use positive voltage output section includes a positive polarity D/A converter and operational amplifier of N-channel MOS transistor input; and negative voltage output section includes a negative polarity D/A converter and operational amplifier of P-channel MOS transistor input in Udo et al apparatus in order to reduce power consumption (See page 1, paragraph 0012 in Udo et al. reference).

5. Claim 7-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Udo et al. in view of Masami et al. (JP 09-212137).

As to claim 7, as best understood by the examiner, Udo et al. teaches an image display device (See page 1, paragraph 0002), comprising: a plurality of scanning signal lines and a plurality of data lines which crossing each other (See Fig. 1, items G1-G4, D1-D6): an electro-optical element (See Fig. 1, item C11), and a switching element (See Fig. 1, item T11) and a pixel capacitor (See Fig. 1, item C11) being provided in each pixel region (See Fig. 1, items G2,

D2) surrounded by adjacent two of plurality of scanning lines (See Fig. 1, items G1, G3) and adjacent two of plurality of data signal lines (See Fig. 1, items D1, D3); a data signal driving circuit for outputting voltages in mutually reverse polarities with respect to a pair of adjacent pixels in direction of data line (See Figs. 1, 2A, items 10, +-, page 2, paragraph 0040).

Udo et al. does not show separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit, separation means being provided between output stage of data signal line driving circuit and data signal line and scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next of a pair, in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair.

Masami et al. teaches separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit (See Figures 1-2, items t1-t2, 101-102, page 3, paragraph 0017), separation means being provided between output stage of data signal line driving circuit and data signal line (See Figure 1, item 102) and scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next of a pair, in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair (See Fig. 1-2, items 101-102, page 2, paragraphs 0014, 0017).

It would have been obvious to one of ordinary skill in the art at the time of invention to use separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit separation means being provided between output stage of data signal line driving circuit and data signal line and scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next of a pair, in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair as shown by Masami et al. in Udo et al apparatus in order to reduce power consumption (See Problem to be solved in Masami et al. reference).

As to claim 8, as best understood by the examiner, Udo et al. teaches an image display device (See page 1, paragraph 0002), comprising: a plurality of scanning signal lines and a plurality of data lines which crossing each other (See Fig. 1, items G1-G4, D1-D6): an electro-optical element (See Fig. 1, item C11), and a switching element (See Fig. 1, item T11) and a pixel capacitor (See Fig. 1, item C11) being provided in each pixel region (See Fig. 1, items G2, D2) surrounded by adjacent two of plurality of scanning lines (See Fig. 1, items G1, G3) and adjacent two of plurality of data signal lines (See Fig. 1, items D1, D3); a data signal driving circuit for outputting voltages in mutually reverse polarities with respect to a pair of adjacent pixels in direction of data line (See Figs. 1, 2A, items 10, +-, page 2, paragraph 0040); separation means for separating an output stage of data signal line driving circuit from data signal line in a blanking period directly before a selection-scanning period of each scanning signal line by a scanning signal line driving circuit, separation means being provided between output stage of

data signal line driving circuit and data signal line (See Fig. 5, items P1-P6, N1-N6, page 3, paragraphs 0054-0055); wherein data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to adjacent pixels in direction of data signal line (See Fig. 2A-2B, page 2, paragraph 0040).

Udo et al. does not show scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next in a pair, in the blanking period directly before the selection-scanning period of the scanning signal line to be scanned first of the pair.

Masami et al. teaches scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next of a pair, in the blanking period directly before the selection-scanning period of the scanning signal line to be scanned first of the pair (See Fig. 1, items 101-102, page 2, paragraph 0014).

It would have been obvious to one of ordinary skill in the art at the time of invention to use scanning signal line driving circuit to carry out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next of a pair, in the blanking period directly before the selection-scanning period of the scanning signal line to be scanned first of the pair as shown by Masami et al. in Udo et al apparatus in order to reduce power consumption (See Problem to be solved in Masami et al. reference).

As to claim 10, Udo et al. teaches an image display device (See page 1, paragraph 0002), which includes in each pixel region (See Fig. 1, items G2, D2) surrounded by adjacent two of plurality of scanning lines (See Fig. 1, items G1, G3) and adjacent two of plurality of data signal lines which cross each other (See Fig. 1, items D1, D3), an electro-optical element (See Fig. 1, item C11), and a switching element (See Fig. 1, item T11) and a pixel capacitor (See Fig. 1, item C11) which correspond to electro-optical element, and which performs a display-driving of electro-optical element by a charge as input in pixel capacitor by switching element (See Fig. 1, item C11, page2, paragraphs 0035-0036); a data signal line driving circuit outputs voltages for gradation display in mutually reverse polarities with respect to adjacent pixels in direction of data signal line (See Fig. 2A-2B, page 2, paragraph 0040).

Udo et al. does not show short-circuit means for short-circuiting a pair of pixel capacitors of pair of adjacent pixels in a selection-scanning period of a previous scanning signal line when scanning by switching polarities for gradation display.

Masami et al. teaches short-circuit means for short-circuiting a pair of pixel capacitors of pair of adjacent pixels in a selection-scanning period of a previous scanning signal line when scanning by switching polarities for gradation display (See Fig. 1, items 101-102, page 2, paragraph 0014).

It would have been obvious to one of ordinary skill in the art at the time of invention to use short-circuit means for short-circuiting a pair of pixel capacitors of pair of adjacent pixels in a selection-scanning period of a previous scanning signal line when scanning by switching polarities for gradation display by Masami et al. in Udo et al apparatus in order to reduce power consumption (See Problem to be solved in Masami et al. reference).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Udo et al and Masami et al. as applied to claim 8 above, and further in view of Hayashi et al. (US Patent No. 6, 130, 654).

Masami et al. teaches control means for controlling to cut off separation means in a blanking period, blanking period being provided directly before selection-scanning period of the scanning signal line to be scanned first of the pair, and to perform the selection-scanning operation of the target pair of scanning signal lines in the cut-off state of separation means (See Fig. 1-2, items 101-102, page 2, paragraphs 0014,
0017).

Udo et al and Masami et al. do not show blanking period at every two horizontal scanning periods.

Hayashi et al. teaches blanking period at every two horizontal scanning periods (See Fig. 8a, items 1H,Vp1, Col. 10, Lines 23-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to use blanking period at every two horizontal scanning periods as shown by Hayashi et al. in Masami et al. and Udo et al apparatus in order to display uniform brightness images (See Col. 1, Lines 44-47 in Hayashi et al. reference).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Hisashi (JP 10-326090) reference discloses refresh circuit which temporarily separates the signal lines and shorts them.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ls

VIJAY SHANKAR
PRIMARY EXAMINER